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10/723,530	11/24/2003	David Lewis	174/304	8666

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,530	LEWIS, DAVID	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,9,16-34,36 and 37* is/are rejected.

7)☒ Claim(s) *5-7, 10-15, 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 8, 16-20, 25-34, 36-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Chaudhary (5,889,411).

Claim 1, Chaudhary shows a logic module circuitry (Fig. 5A) comprising:

combinational logic circuitry having at least first (H, Fig. 5A), second (J, Fig. 5A), and third stages (82H and 82J), each of said stage responsive at least one input of the logic module (J1-J4, H1-H4, BJ, BH, CE1, CK1, SR1); and

XOR circuitry (SH or SJ) interposed between the third stage and an output of the combination logic circuitry (ZQ or VQ), the XOR circuitry receiving at one input a carry in signal (CIN1) and at another input (O from J or H) an output signal of one of the stages of the combinational logic circuitry.

Claim 2, Chaudhary shows the circuitry defined in claim 1 further comprising: programmably controlled circuitry (CA) for selectively disabling (CIN1 not selected is considered as disabling) the carry in signal.

Claim 3, Chaudhary shows the circuitry defined in claim 1 further comprising: circuitry (CJ or CH) for producing a carry out signal (COUT 1) from the carry in signal (CIN1) and combinational signals (82J or 82H) in the combinational logic circuitry.

Claim 4, Chaudhary shows the circuitry defined claim 3 wherein the circuitry for producing comprises: multiplexer circuitry (CJ or CH is a multiplexer) for using a first of the combinational signals (O from J or H) to control selection of one of the carry in signal (CIN1) and a second of the combinational signals (82J or 82H) as the carry out signal.

Claim 8, Chaudhary shows the circuitry defined in claim 1 wherein the combinational logic circuitry has first (H), second (J), third (82H and 82J), and fourth stages (DH and HJ), and wherein the XOR circuitry (SH or SJ is between 82H, 82J and DH, HJ) is interposed between the third and fourth stages.

Claim 16-18, Chaudhary shows the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic sum, difference, and product of first and second stage input signals (inherent limitations of a look-up table which is configurable to perform any desired logic functions, also see col. 6, lines 10-12).

Claim 19, Chaudhary shows the circuitry defined in claim 18 wherein the third stage and the XOR circuitry are operable to form the arithmetic sum of the output signal (Z or V), a third stage input signal (H1 and H1), and a carry in signal (CIN1).

Claim 20, Chaudhary shows a programmable logic device (FPGA) comprising logic module circuitry as defined in claim 1.

The apparatus described above in claims 1, 16-18, is applicable to the method claims 25-26, and 29.

Claim 27, Chaudhary shows the method defined in claim 26 wherein the using comprises: employing the XOR circuitry (SH or SJ) to produce a further arithmetic sum (col. 6, lines 10-12) of the output signal and the carry in signal (CIN1).

Claim 28, Chaudhary shows the method defined in claim 27 further comprising: additionally programming the first and second stages so that they can produce signals for use in providing a carry out signal (COUT1) that results from an arithmetic summation of the first and second stage input signals (output O from H and J which controlling CJ) and the carry in signal (CIN1).

Claim 30, Chaudhary shows the method defined in claim 29 further comprising: using the third stage (82H and 82J) and the XOR circuitry (SH and SJ) to form an arithmetic sum of the output signal (col. 6, lines 10-12), the carry in signal (CIN1), and a third stage input signal (H1, H2, J1, J2).

Claim 31, Chaudhary shows the method defined in claim 30 further comprising: additionally programming the first and second stages so that they can produce signals for use in providing a carry out signal (COUT1) that results from an arithmetic summation of the output signal (output O from H and J controlling CJ), the carry in signal (CIN1), and the third stage input signal (J1, J2).

Claim 32, Chaudhary shows logic module circuitry (5A) comprising:

look-up table circuitry (look-up table, col. 4, lines 16) having first (H), second (J), third (DJ and DH), and fourth stages (RV and RZ); and

XOR circuitry (SJ) receiving at one input a carry in signal (CIN1) and at another input signal information from a source stage (J), the XOR circuitry producing further

signal information applied to a destination stage (DJ), wherein the source stage is selected from the group consisting of second (J) and third stages, and wherein the destination stage is the third stage (DJ) if the source stage the second stage, and the destination stage the fourth stage if the source stage is the third stage.

Claim 33, Chaudhary shows the circuitry defined in claim 32 further comprising: circuitry (CA) for selectively disabling (CIN1 not selected) the carry in signal.

Claim 34, Chaudhary shows the circuitry defined in claim further comprising: circuitry (CJ) for producing a carry out signal (COUT1) from at least the carry in signal (CIN1) and signal information from the source stage (O from J).

Claim 36, Chaudhary shows The circuitry defined in claim 32 wherein the look-up table circuit leading to the XOR circuitry includes circuit elements (inherent elements of programmable look-up table) that are programmable so that the signal information from the source stage that the XOR circuitry receives is indicative of a result of arithmetically adding (addition, col. 6, lines 10-12) together first and second stage input signals.

Claim 37, Chaudhary shows the circuitry defined in claim wherein the look-up table circuitry leading to the XOR circuitry includes circuit elements (inherent elements of programmable look-up table) that are programmable so that the signal information from the source stage that the XOR circuitry receives is based at least in part on a result of arithmetically multiplying (multiplication, col. 6, lines 10-12) first and second stage input signals.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Rupp (6,633,181).

Claim 1, Rupp shows a logic module circuitry (404, Fig. 7) comprising:

combinational logic circuitry having at least first (702), second (704), and third stages (710), each of said stage responsive at least one input of the logic module (CM, FE, AF, AE, Ki); and

XOR circuitry (916, Fig. 9 which is 706 in figure 7) interposed between two stages, the XOR circuitry receiving at one input a carry in signal (Ki, col. 6, line 32) and at another input (P, Fig. 9) an output signal of one of the stages of the combinational logic circuitry.

Claim 2, Rupp shows the circuitry defined in claim 1 further comprising: programmably controlled circuitry for selectively disabling the carry in signal (914, Fig. 9 and col. 6. lines 58-67).

Claim 9, Rupp shows the circuitry defined in claim 1 wherein the XOR circuitry (916) is interposed between the second (704, Fig. 7) and third stages (710).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaudhary (5,889,411) in view of Park et al (6,359,468).

Chaudhary discloses the claimed invention except for a memory, processing circuitry, and programmable logic device mounted on a printed circuit board.

Park discloses a memory, processing circuitry, and programmable logic device mounted on a printed circuit board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the programmable logic device of Chaudhary in a digital processing system of Park, in order to provide wide variety of applications where the advantage of using programmable logic device.

Allowable Subject Matter

5. Claims 5-7, 10-15, and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

-a first path at a relatively high speed and a second at less than the relatively high speed.

-the third stage has first and second combinational signal outputs, and wherein the XOR circuitry logically combines the first combinational signal output with the carry in signal to produce a sum output signal.

-the first and second stages having first, second, third, and fourth combinational signal outputs, and wherein first XOR circuitry logically combines the carry in signal with the first combinational signal output and second XOR circuitry logically combines the carry in signal with the second combinational signal output to produce two further signals for application to the third stage.

-the circuitry for producing is connected so that the carry out signal is based in part on a third stage input signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/4/06

ANH Q. TRAN
PRIMARY EXAMINER